PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P16854-dbo	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/EP 02/10073	International filing date *(day/month/year)* 09.09.2002	Priority date *(day/month/year)* 09.09.2002
International Patent Classification (IPC) or both national classification and IPC H03M13/27		
Applicant TELEFONAKTIEBOLAGET LM ERICSSON (PUBL) ET AL.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
16.02.2004	10.12.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Barel-Faucheux, C Telephone No. +49 89 2399-2516

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP 02/10073

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-46 as originally filed

Claims, Numbers

1-20 as originally filed

Drawings, Sheets

1-7 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	5 6 8 10 15 16 18-20
	No:	Claims	1-4 7 9 11-14 17
Inventive step (IS)	Yes:	Claims	8 18-20
	No:	Claims	5 6 10 15 16
Industrial applicability (IA)	Yes:	Claims	1-20
	No:	Claims	

2. Citations and explanations

   see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following documents:

D1: EP-A-1 111 797 (MATSUSHITA ELECTRIC IND CO LTD) 27 June 2001 (2001-06-27)

D2: EP-A-1 195 910 (SAMSUNG ELECTRONICS CO LTD) 10 April 2002 (2002-04-10)

1. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1 to 4, 11 to 14, is not new in the sense of Article 33(2) PCT.

1.1. The document **D1** discloses a method for interleaving, according to an interleaving scheme ("MIL pattern": see page 2, line 10, to page 3, line 19, and figures 1, 2) , an input sequence ("In(x)") comprising K>=2 bits into an interleaved sequence, said method including the steps of (figures 3, 4; page 4, line 5, to page 5, line 2):

a) storing the input sequence in a first memory means (figure 3: "input memory" (101)),
b) generating first indices (figure 4: "r+R*c"; "r", "c") of N succeeding bits of the interleaved sequence, wherein N is selectable from values in the range of 1,2,..,K.
c) converting according to an inverse of said interleaving scheme, said first indices into second indices (figure 4: "C*Mil_row[r]+Mil_col[c]"; "Mil_row[r]", "Mil_col[c]") indicative of the positions where said N succeeding bits of the interleaved sequence are stored in said first memory means when they are stored therein,
d) reading out said N succeeding bits from said positions in said first memory means, thereby generating at least part of said interleaved sequence.

Thus claim 1 is not new.
This applies also to corresponding interleaving unit claim 11.

1.2. Furthermore in **D1**,
- said first memory means is organized in a matrix form comprising rows and columns,
- said first indices comprise first row indices (r) and first column indices (c),
- said second indices comprise second row indices (Mil_row[r]) and second column indices (Mil_col[c]),

and wherein said step of converting includes:
- converting said first row indices (r) into said second row indices (Mil_row[r]) so that

inter-row permutation operations according to said interleaving scheme are performed when said step of reading out is executed (page 4, lines 11-15),
- converting said first column indices (c) into said second column indices (Mil_col[c]) so that intra-row permutation operations according to said interleaving scheme are performed when said step of reading out is executed (page 4, lines 17-20).

Thus claim 2 is not new.
This applies also to corresponding interleaving unit claim 12.

1.3. Moreover in the method of **D1**, said step of converting said first row indices includes:
- storing at least one permutation pattern ("row pattern") defining said inter-row permutation operations in a second memory means ("row pattern memory" (102)),
- addressing said second memory means with addresses depending on at least said first row indices, thereby causing said second memory means to output said second row indices (page 4, lines 11-15).

Thus claim 3 is not new.
This applies also to corresponding interleaving unit claim 13.

1.4. Moreover in the method of **D1**, said step of converting said first column indices includes (page 4, lines 33-40):
- converting said first column indices (c) and said second row indices (r) into said second column indices (Mil_col[c]) so that intra-row permutation operations depending on a row index are performed when said step of reading out is executed.

Thus claim 4 is not new.
This applies also to corresponding interleaving unit claim 14.

2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 5, 6, 15 and 16, does not involve an inventive step in the sense of Article 33(3) PCT.

2.1. The additional feature of claim 5 with respect to claim 4 to which it refers is that said first column indices includes:
- determining base sequence indices (Zrb(ca)) depending on said first column indices (ca) and said second row indices (rb) by adding index increments (krb) depending on

said second row indices (rb) to previously determined base sequence indices (Zrb(ca-1)),
- determining said second column indices (cb) on the basis of at least said first column indices (ca) and said base sequence indices (Zrb(ca)).

2.2. The problem to be solved here may therefore be regarded as providing a means to simplify the operations of the hardware when calculating the intra-row permutation pattern.

2.3. The solution proposed in claim 5 of the present application cannot be considered as involving an inventive step (Article 33(3) PCT) for the following reasons:

2.3.1. Zrb(ca) of the present application is given by Equation (10) on page 35. This is identical to Uj(i) given by Equation (3) on pages 3 and 4 of **D2** or Equation (8) on page 7 of **D2** with the following corresponding notations :

auxiliary parameter Zrb(ca) in the Application corresponds in **D2** to intra-row permutation pattern Uj(i),
base sequence c() in the Application corresponds in **D2** to the intra row permutation basic sequence s(),
ca in the Application corresponds in **D2** to i,
p() in the Application corresponds in **D2** to r(),
rb in the Application corresponds in **D2** to j,

Moreover in the application index increments krb is identical according to equation (12) to r(j) mod (p-1) in **D2** (see **D2**: page 6, lines 56, to page 8, line 14 and Equations (8) and (9)).

2.3.2. When seeking to simplify the operations of the hardware, the person skilled in the art will reconsider the intra-row permutation patten calculation thereby arriving at document **D2** which seeks to solve the same problem of interleaving operations, and will straightforward replace the (multiply, mod) operation by a recursive operation using an increment value.

2.4. Thus claim 5 is not inventive. This applies also to claim 15.

2.5. The additional features of claim 6 with respect to claim 5 to which it refers are also known from **D2** wherein said step of converting includes (figure 2; page 5, line 52, to

page 8, line 15):
- storing at least said index increments in a third memory means ("incr(j) memory" (210)),
- storing at least one base sequence specified by said interleaving scheme in a fourth memory means ("intra-row permutation pattern storage arrangement" (206)),
wherein
- said step of determining base sequence indices is adapted to address said third memory means so as to read therefrom said index increments,
- said step of determining said second column indices is adapted to address said fourth memory means so as to read therefrom corresponding values of said at least one base sequence.

Thus claim 6, and corresponding interleaving unit of claim 16, are not inventive.

3. The additional feature of claim 7 (respectively interleaving unit of claim 17) with respect to the previous claims which it refers, are that N is selected to have a value of K, and that said first memory means is adapted to generate said interleaved sequence when said N succeeding bits are read out from said positions.
This is not new.

4. The additional feature of claim 9 with respect to the previous claims which it refers is that said steps of generating and converting are executed at least partially, before said step of storing. This is also known from **D1**, where the address in the matrix are calculated before storage.

5. The additional feature of claim 8 (respectively interleaving unit of claim 18) with respect to the claims to which it refers is that N is selected to have a value of essentially K/M with M>=2 denoting a sub-sampling factor, and wherein said first memory means is adapted to generate an output sequence representing one of M polyphases of said interleaved sequence when said N succeeding bits are read out from said positions.

Claim 19 defines an interleaving apparatus for interleaving, according to an interleaving scheme, an input sequence comprising K>=2 bits into an interleaved sequence, including:
- M>=2 interleaving units according to claim 18, each adapted to receive said input sequence and to generate an output sequence representing a different one of said M polyphases,
- a combiner connected to said M interleaving units for combining the output sequences

generated by said M interleaving units into said interleaved sequence,
- a control unit for controlling the operations of said M interleaving units and said combiner.

whereas claim 20 defines Interleaving apparatus according to claim 19 including;
- fifth memory means, connected to said M interleaving units, for storing at least one of a complete set of base sequences according to the interleaving scheme and a complete set of base sequence index increments (krb).

These features of claim 8, 18, 19 and 20 is neither known from, nor rendered obvious by, the available prior art.